Vertical Bloch Line (VBL) Storage Technology*

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VBL Technology Presentation Overview

- ■ A Solid-State Storage Myth
- ■ Technology Attributes
- ☐ Technology Architecture
- ■ Technology Status

The solid-state storage myth

- The myth: Providing solid-state storage ~~must~~ always be expensive:
  - It is often assumed that solid-state storage must be expensive on a per-bit basis.
  - It is often assumed that mechanical technologies, such as disk and tape, must be less expensive.
- The basis for the myth:
  - Alternative (non-VBL) solid-state technologies are often costly:
    - —Fabrication processes are often costly/exotic.
    - —Yields are low.
  - Alternative solid-state technologies often offer low performance:
    - —Low chip capacities (64 kbits-1 Mbit).
    - —Performance limitations:
      - 0 Poor reliability.
      - 0 Slow write/erase rates.
      - 0 Limited cyclability.
      - 0 Other limitations.
  - . Thus high cost per bit and reduced market competitiveness often result.

VBL technology opportunity against the solid-state storage myth

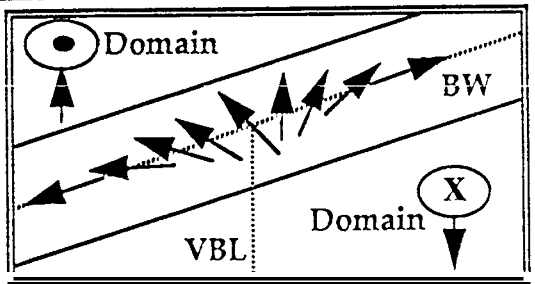
- VBL technology opportunity:
  - VBL technology has inherent attributes that can make it less expensive to produce than today's DRAM, disk, and tape costs:
    - —High bit density.
    - —Low fabrication costs:
      - O Simple and high-yield fabrication processes.
      - O Simple and high-yield device design structures.
      - O Standard Czochralski substrate wafer growth.
- ❑ Achieving functionality at high volume and high yield is the key.

VBL Technical Background Technology Opportunity

- VBL technology Potential uniquely and simultaneously offers many desirable data storage attributes in a single technology:
  - **High areal storage density: >1 Gbit per chip.**
  - **High volumetric storage density: 1 Gbit/cm^3 to >1 Tbit/cm^3.**
  - **Solid-state form.**
  - **Nonvolatility.**
  - **Radiation hardness.**
  - **Scalability for future technology advancement.**
  - **Dual-usability.**
  - **Mass data erasability.**
  - **No material fatigue limitations.**
  - **Near-term availability.**
- VBL capabilities can enable new data system concepts and applications:
  - **SolId-State Recorders**
  - **Solid-State Disks**
  - **Local storage for processor nodes**
  - **Buffer Storage**
  - **Archival storage**

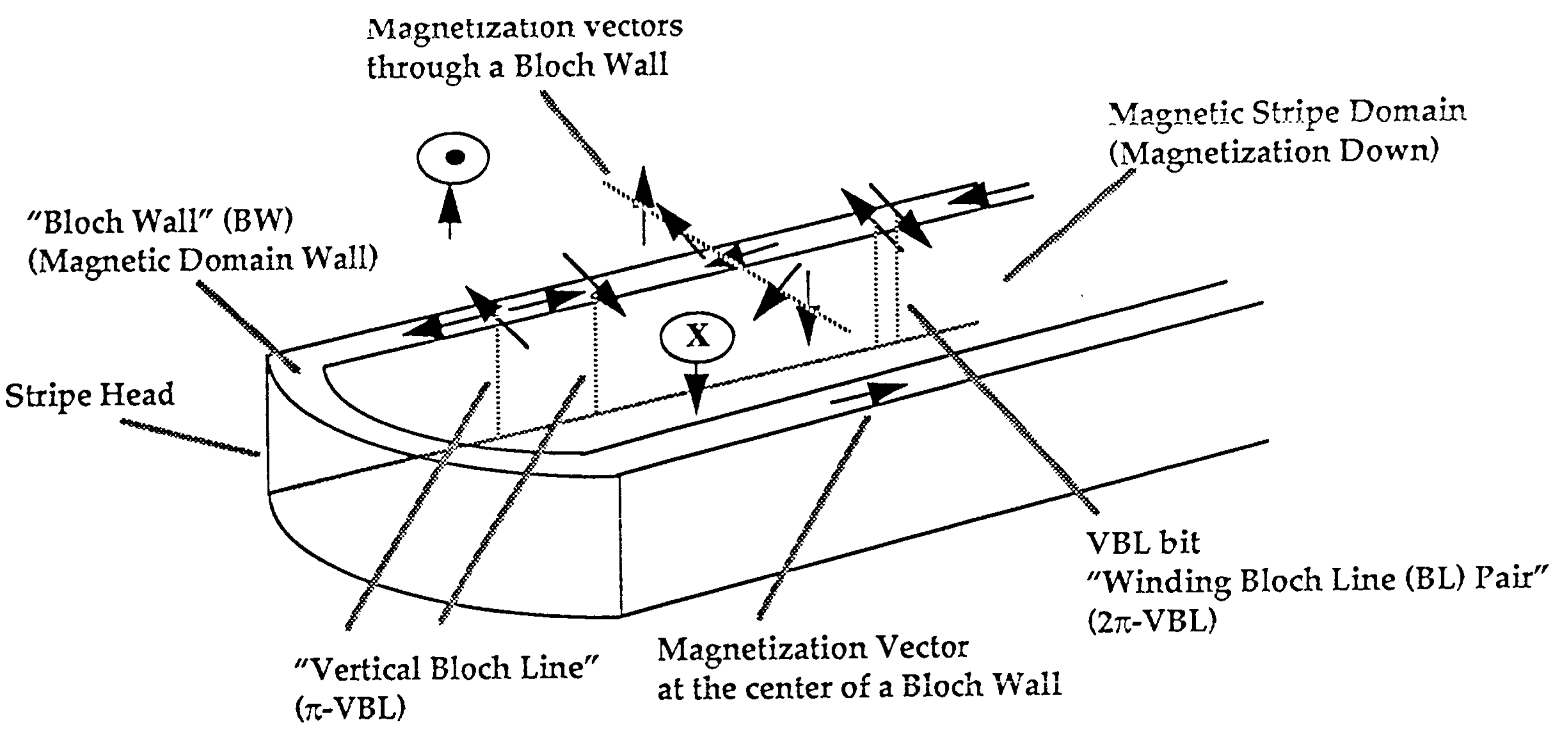
Magnet•c Domain Structure: Background

Close-up of the magnetization vectors through a Bloch Line in a Bloch Wall.

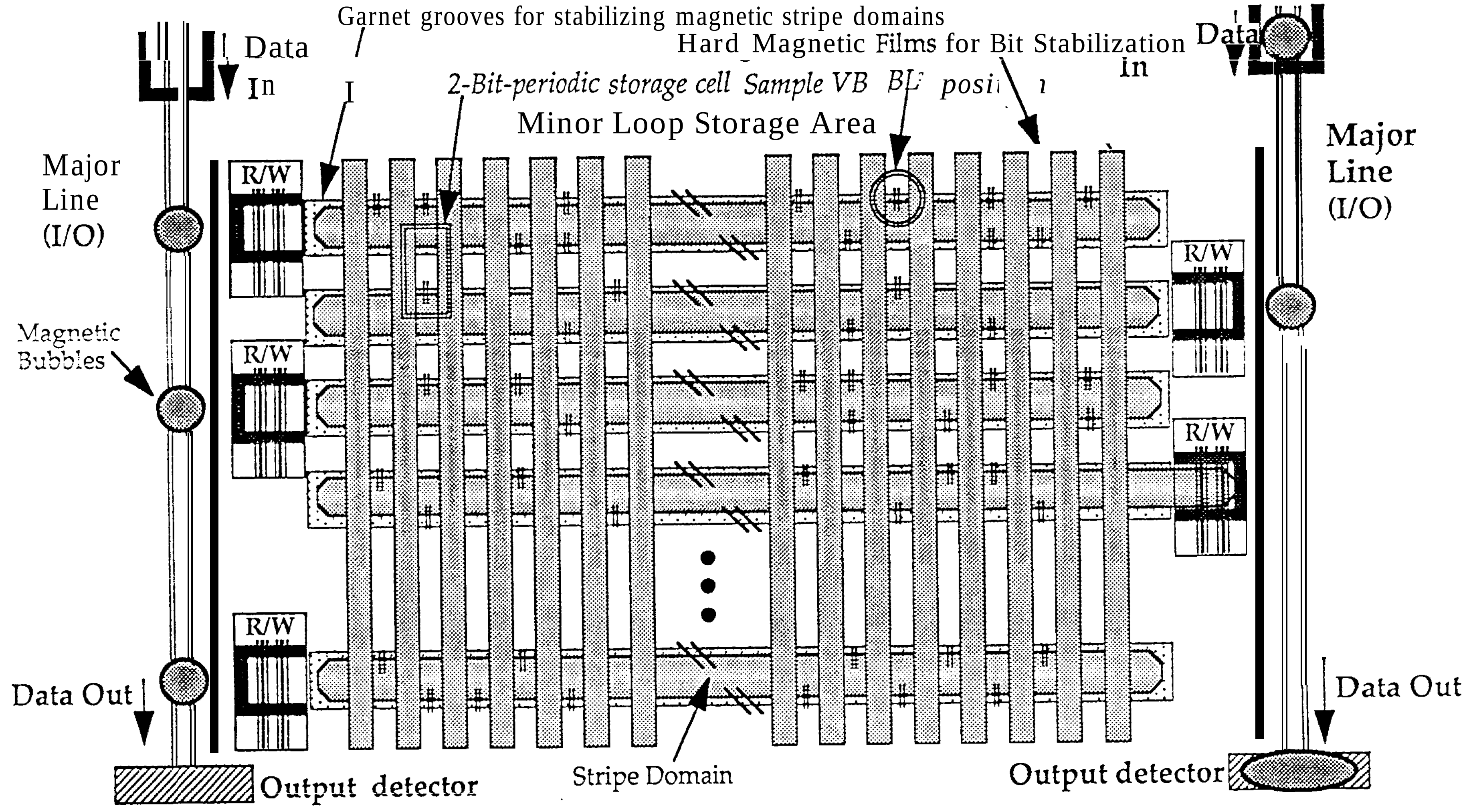


A=Exchange constant; K_u=Perpendicular anisotropy constant;
K_p=In-plane anisotropy constant; M=Magnetization.
Thickness, straight BW = $\Delta_0 = \pi(A/K_u)^{1/2}$
Energy density, straight BW = $\sigma_0 = 4(AK_u)^{1/2}$
Thickness, BW w/ periodic array (s) of BLs= $\Delta_* = \Delta_0[1+(\pi\Delta_0/s)^2+(2Q)^{-1}]^{-1/2}$
Energy density, Bloch Wall w/ periodic array of BLs: $\sigma_* = \sigma_0[1+(\pi\Delta_0/s)^2+(2Q)^{-1}]^{1/2}$
Thickness, single BL: $\pi(A/|2\pi M^2 \pm K_p|)^{1/2}$
$Q = K_u/2\pi M^2$

A magnetic domain with domain wall structure:



A VBL Storage Chip Architecture



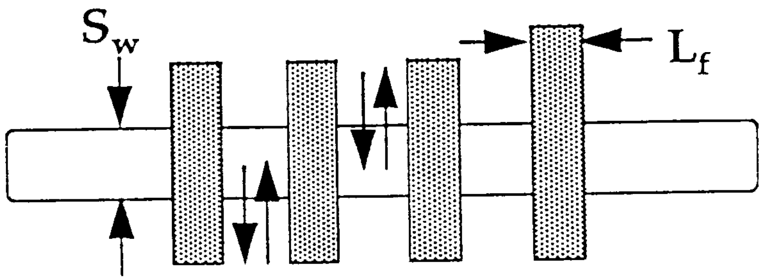
VBL Storage Chips: Areal Storage Density Performance

	$L_f = 1\ \mu m$	$L_f = 0.5\ \mu m$	L_f = 0.1 urn
S*= 5 µm	10 Mbits/cm^z	20 Mbits/cm^z	100 Mbits/cm^2
S*= 2 µm	25 Mbits/cm^z	50 Mbits/cm^z	250 Mbits/cm^z
S_w = 1 µm	50 Mbits/cm^z	100 Mbits/cm^z	500 Mbits/cm^z
S_w = 0.5 urn	100 Mbits/cm^z	200 Mbits/cm^z	1,000 Mbits/cm^z
S_w = 0.25 µm	200 Mbits/cm*	400 Mbits/cm^z	2,000 Mbits/cm^z

VBL Memory areal storage density is proportional to:

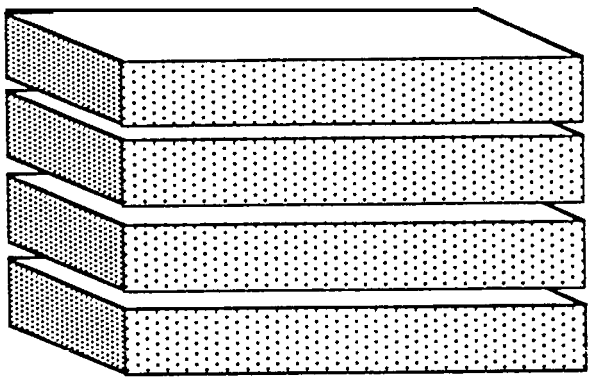
$$1/((S_w) \times (L_f))$$

Stripe:



VBL Storage Chips: Volumetric Storage Performance

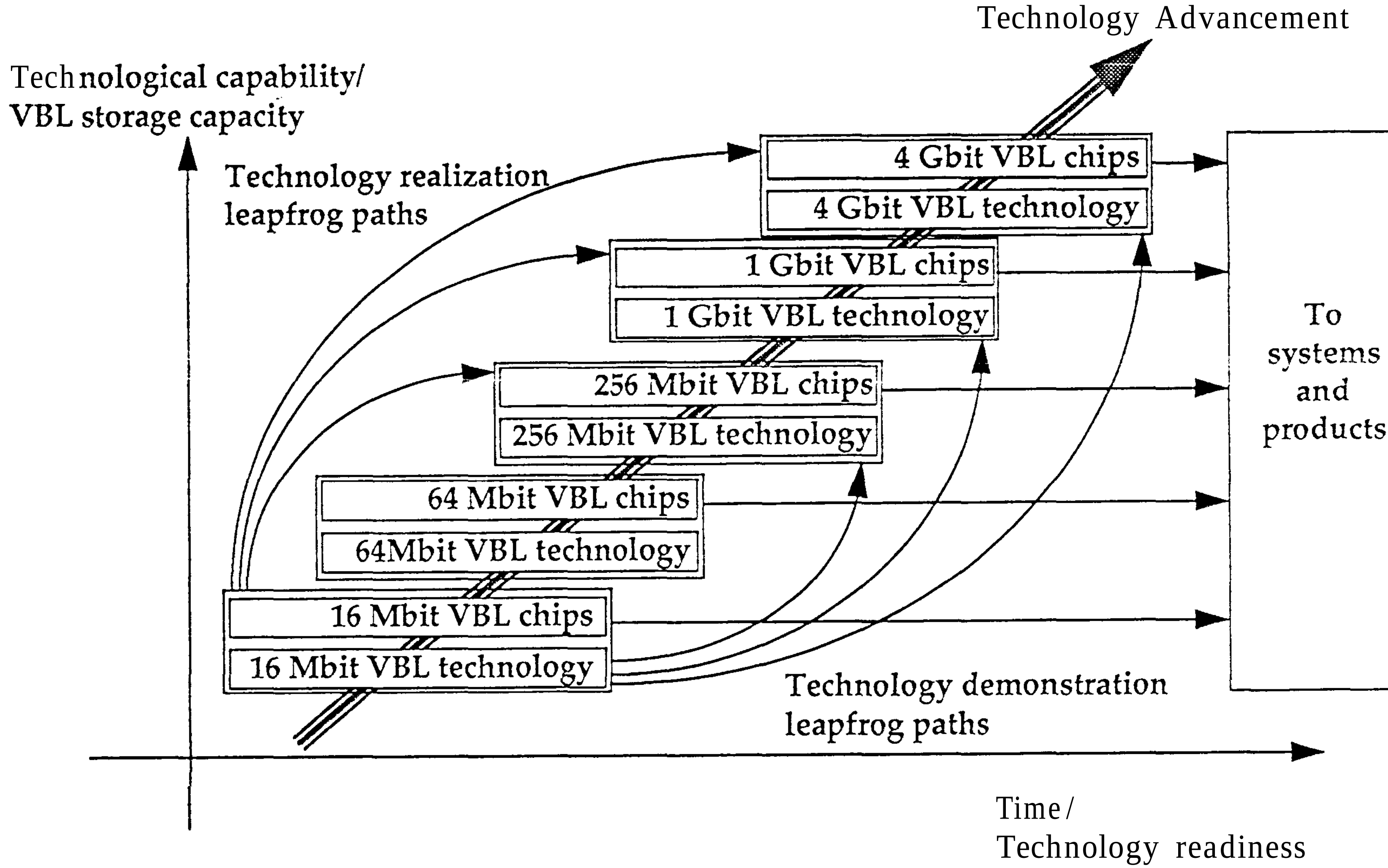
Areal Storage Density	Chip Die Density: 16 die/cm (25 mils/die) (625 µm/die)	40 die/cm (10 mils/die) (250 µm/die)	200 die/cm (2 mils/die) (50 µm/die)	400 die/cm (1 mil/die) (25 µm/die)
25 Mbits/cm²	0.4 Gbits/cc	1 Gbit/cc	5 Gbits/cc	10 Gbits/cc
100 Mbits/cm²	1.6 Gbits/cc	4 Gbits/cc	20 Gbits/cc	40 Gbits/cc
200 Mbits/cm²	3.2 Gbits/cc	8 Gbits/cc	40 Gbits/cc	80 Gbits/cc
1,000 Mbits/cm²	16 Gbits/cc	40 Gbits/cc	200 Gbits/cc	400 Gbits/cc
10,000 Mbits/cm²	160 Gbits/cc	400 Gbits/cc	2,000 Gbits/cc	4,000 Gbits/cc



3D VBL Chip Stack

Chip Die Period

VBL
Technology Advancement Path



VBL Technology
Near Term Development Goals

- **Solid-state, nonvolatile chips:**
  - **16 Mbits, 64 Mbits, and/or 256 Mbit chips.**
  - **2 Gbits per cubic centimeter in 3D packaging.**
  - **300 Gbits per kg in 3D packaging.**
- Data rates:
  - 0 to >40 Mbit/sec **per** chip.
  - >1 Gbit/sec **per system.**
- Power consumption:
  - < 10 mW **per Mbit/see during input/output operations.**
  - < [illegible] mW per **active chip during bit propagation operations.**
- **Applicability:**
  - **Ruggedizable.**
  - Space qualifiable.
  - Commercializable.

Potential VBL Production Cost Advantage

- VBL technology can be cheaper to produce per bit than any present IC technology:
  - **Wafer fabrication costs can be lower.**
  - **Substrate fabrication costs reduce with volume applications.**
- VBL comparisons to semiconductor processing:
  - **VBL has no pn junction issues:**
    - **—VBL is less sensitive to contamination.**
    - **—VBL is less sensitive to impurities.**
  - **VBL has no interlayer contacts (vias) in the memory storage array.**
  - **VBL has no polysilicon and no gate oxide (big CMOS issues).**
  - **VBL fabrication requires no special processing equipment.**
  - **Lithography:**
    - **—VBL has more bits/cm^2 with the same design rules.**
    - **—Bit density more tolerant to alignment errors.**
    - **—Long, parallel lines ideal for future x-ray and holographic lithography.**
  - **VBL has fewer mask steps than CMOS.**
  - **VBL energy stored per bit stays constant as bit size shrinks.**

VBL Technology Status

❑ Features which have been demonstrated:

- Bubble propagation in the major line.
- Stripe chopping for readback.
- Stripe expansion for writing.
- Partial grooving stripe stabilization.
- Permanent magnet bit cell formation
- Ability to match bias fields in chip to realize a single chip operating point.
- VBL observability.
- Computer simulation capabilities.

■ Features to be demonstrated:

- A fully integrated storage device with good margins, including:
  - —Integrated write/read gates.
  - —Integrated input/output data line with signal detector.
  - —Active bit definition.

■ Features needing demonstration:

- Storage density upper limits.
- Maximum data access and transfer rates.
- Minimum power performance.

VBL Conclusions

- VBL technology potentially offers a variety of desirable data storage technology attributes for a variety of applications.
- VBL technology potentially offers high market volume and effective cost performance potential.
- Near-term development plans are intended to develop VBL technology to realize technological potential.